BOSSHARD ELEKTRONIK

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ispLSI5256VA - Demoboard

User Manual

Version 1.1

We are aware of the fact, that very few designers read manuals. Nevertheless we recommend to read this manual before starting to work with the demoboard. A lot of FAQ's are answered here.

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Bosshard Elektronik, Undelstrasse 48, CH-8493 Saland, Switzerland
Tel. +41 (0)52 394 13 13; Fax +41 (0)52 394 13 14; www.bosshard-elektronik.ch

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0. Kit Contents

Please check the contents of the box when receiving the demoboard. It should contain the following items:

- ispLSI5256VA - Demoboard
- Application example description
- This Manual
- The schematic of the board

We do not ship any software with the board. The application-examples can be downloaded from our website (www.bosshard-elektronik.ch)

1. Introduction

This demoboard was designed to give an easy access to the features of the Lattice 5kVA-Family for design engineers. The popularity of this CPLD-family is growing rapidly. Please refer to Lattice documentation or homepage for more details on the architecture and capabilities of this device family.

The board can be used for prototyping as well as for design-verification, performance tests, education purposes, evaluation of the 5kVA CPLD family or simply to play around with it and have some fun.

2. Features

- Equipped with an ispLSI5256VA-100LB208. Translation: In-System programmable 3.3V-CPLD with 256 Macrocells, specified to run at max. 100MHz in a BGA208 package.
- On-board 3.3V voltage-regulator
- On-board oscillator running at 4MHz
- All device-pins are available on standard single or double row headers
- Prototyping area for your own circuitry
- In-System programmable via JTAG-Port. Use the Lattice Download-Cable for direct download from the PC parallel-port to the demoboard.
- 4 Digit LED display
- User switches connected to CPLD:
  - 4 User-Keys
  - Reset-Key
  - 8 DIP-switches

3. Board Layout

Use figure 1 to locate the different components on the board.

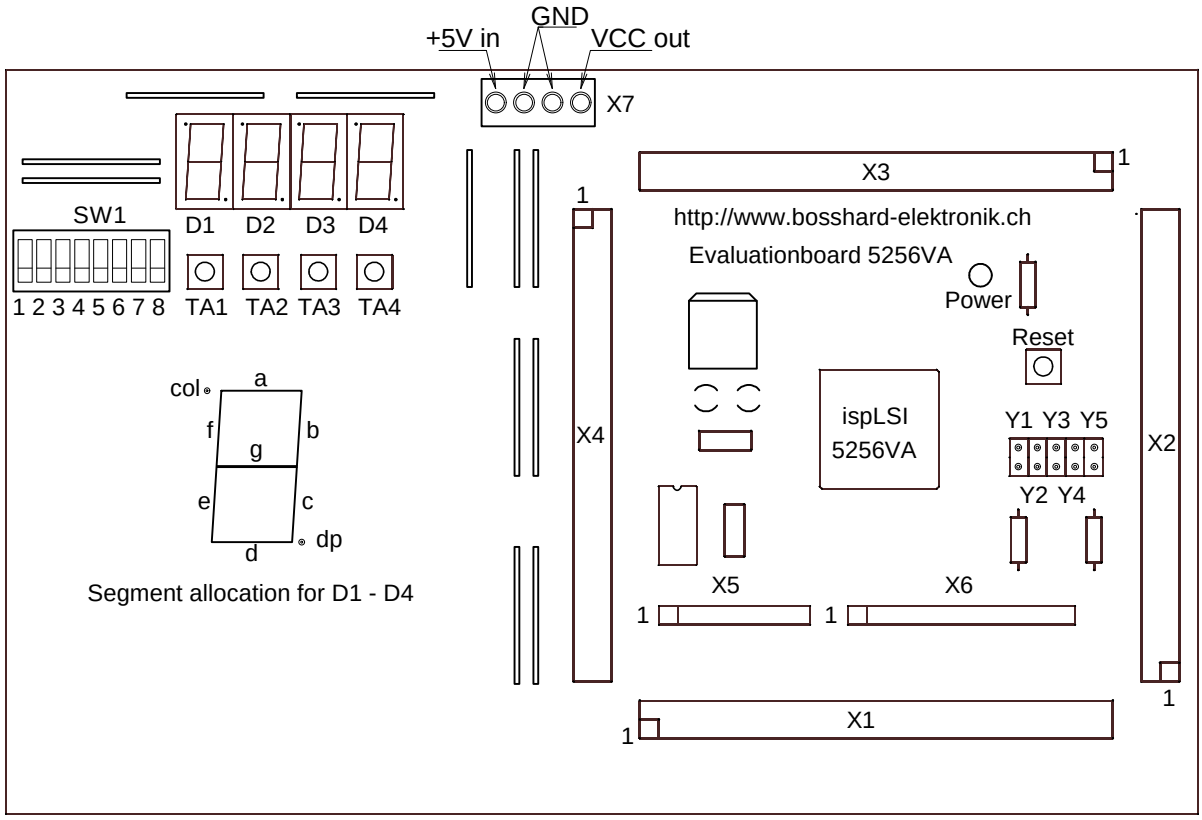

Figure 1. ispLSI5256VA Demoboard Layout

4. Power Supply

The board needs a 5 Volt / 1A power-supply. The on-board regulator generates the needed 3.3V, which is available at X7 for use in other peripherals.

The power consumption of the ispLSI5256VA depends mainly on your JEDEC-file and the clock frequency. This varies the current available from the 3.3V output, but even in worst case you can draw 100mA. The onboard voltage regulator is overcurrent- and overtemperature-protected.

The ispLSI5256VA supports 2.5V VCCIO, which need to be supplied externally. Jumper Y1 connects VCCIO to the 3.3V-supply. Jumper Y2 connects the VCCIO device pin to X6, Pin 11.

REMARK: To clarify the VCCIO-issue: It is optional to supply 2.5V for VCCIO and is only needed, when you want to interface to 2.5V - components.

CAUTION: Do not feed external 2.5V with Jumpers Y1 and Y2 both set! Set Y1 for VCCIO = 3.3V (from on-board supply) or set Y2 for VCCIO = 2.5V (connect a 2.5V / 30mA - supply to X6, Pin 11).

5. Clocks, Output Enables and Reset/Preset

All clocking options available from the ispLSI5256VA are usable on this board. For test-applications an on-board oscillator running at 4MHz is connected via jumper Y3 to the CLK2 - pin. Figure 3 shows the clock structure of the device. You can see here, why we chosen CLK2 for the onboard clock - it's the most flexible one because it can be used inverted (internal clock-line CLK2) and non-inverted (internal clock-line CLK3) at the same time. In case the clock-signal is used in product-terms the CLK2-pin is configured as I/O –pin by software.

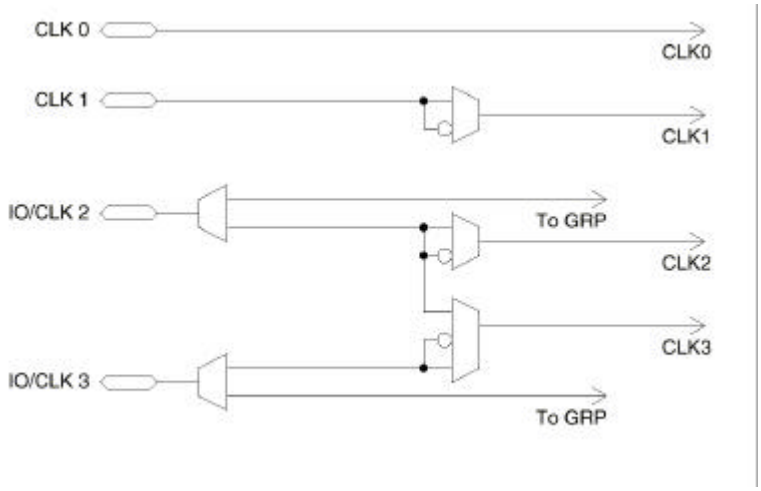

Figure 3. ispLSI5256VA clock structure

Jumper Y4 connects the CLK2 pin to X6, pin 5. If you want to feed an external clock to CLK2 or use it as I/O, set jumper Y4 and remove jumper Y3.

CAUTION: Do not feed an external clock signal to X6, pin5 with both Y3 and Y4 set. You will probably kill your clock source, the onboard-oscillator or both!

All connections for X6 are listed in table1.

Device-pin	X6 pin	Remark
VCC	1	
GND	2	
CLK0	3	Use for fast clock
CLK1	4	
CLK2 / IO 89	5	Connected via Y4 to X6, via Y3 to onboard osc.
CLK3 / IO 98	6	
GSET/GRST	7	On-board RESET-button pulls this pin to GND, a 10kΩ pull-up is connected to this pin
TOE / IO 0	8	Jumper Y5 pulls this pin to GND
GOE0	9	General Output Enable 0
GOE1	10	General Output Enable 1
VCCIO	11	Connected via Y2
GND	12	

Table 1. X6 connections

6. I/O Connections, LED, Switches and pushbuttons

All I/O-pins are connected to the headers. The connections are listed in tables 2,3,4 and 5. Every I/O can be selected to run at VCC (3.3V) or VCCIO (2.5V, externally supplied to VCCIO-Pin) by software. Choosing I/Os to run at VCCIO with a floating VCCIO-Pin is not specified in the ispLSI5256VA - datasheet and will show an unpredictable behavior.

HINT: Inputs, that run on 3.3V can be driven with a 5V-signal. Outputs are 5V TTL - compatible. To achieve 5V CMOS compatible output-levels, select the open-drain option for the output (in the software) and add an external pull-up.

The board features four 7-Segment LED displays with decimal point (dp) and colon (col). The LED segments are ON when the device-pin is driven LOW. Figure 4 shows the segment allocation.

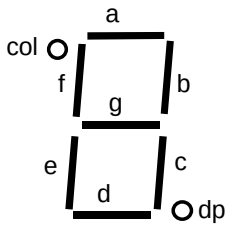

Figure 4. LED display segment allocation

The switches SW1 .. SW8 and the pushbuttons TA1 .. TA4 pull the corresponding I/O-pin to GND when switched on or pushed. A 10kΩ pull-up resistor is connected to all of these signals to ensure a logic high on the pin, when the switch is in off position or the pushbutton is not pressed.

When connecting external signals to X1, pins 4..19, please take in account these pull-ups. When connecting external signals to X4, your signal-source has to be able to sink approx. 7 mA (current through LED-segments) to drive logic low.

X1 Pin	Device Pin	Function		X1 Pin	Device Pin	Function
1		VCC		26		GND
2		GND		27	R4	
3	NC			28	R5	
4	L2	TA4		29	P5	
5	L1	TA3		30	T2	
6	L3	TA2		31	R6	
7	M1	TA1		32	T3	
8	M2	SW7		33		VCC
9		VCC		34		GND
10		GND		35	T4	
11	M3	SW8		36	T5	
12	N1	SW6		37	R7	
13	N3	SW5		38	P6	
14	N2	SW4		39	T6	
15	P2	SW3		40	T7	
16	P1	SW2		41		VCC
17		VCC		42		GND
18		GND		43	R8	
19	R1	SW1		44	P8	
20	R2			45	P7	
21	R3			46	T8	
22	P3			47	T9	
23	T1			48	R9	
24	P4			49		VCC
25		VCC		50		GND

Table 2. X1 Pin connections

X2 Pin	Device Pin	Function		X2 Pin	Device Pin	Function
1		VCC		26		GND
2		GND		27	R16	
3	R10			28	P16	
4	T10			29	N15	
5	T11			30	N14	
6	T12			31	M14	
7	T13			32	N16	
8	T14			33		VCC
9		VCC		34		GND
10		GND		35	M15	
11	P11			36	M16	
12	P12			37	L14	
13	R11			38	L15	
14	T15			39	L16	
15	T16			40	K14	
16	R14			41		VCC
17		VCC		42		GND
18		GND		43	K15	
19	R12			44	K16	
20	P14			45	J14	
21	P13			46	J15	
22	R13			47	J16	
23	R15			48	H16	
24	P15			49		VCC
25		VCC		50		GND

Table 3. X2 Pin connections

X3 Pin	Device Pin	Function		X3 Pin	Device Pin	Function
1		VCC		26		GND
2		GND		27	C13	
3	G16			28	A14	
4	F14			29	C12	
5	G15			30	B12	
6	F16			31	A13	
7	E14			32	A12	
8	F15			33		VCC
9		VCC		34		GND
10		GND		35	C11	
11	E16			36	B11	
12	D16			37	NC	
13	C16			38	B10	
14	B16			39	A10	
15	D15			40	C10	
16	D14			41		VCC
17		VCC		42		GND
18		GND		43	B9	
19	A16			44	C9	
20	C15			45	A9	
21	B15			46	A8	
22	A15			47	C8	
23	B14			48	C7	
24	NC			49		VCC
25		VCC		50		GND

Table 4. X3 Pin connections

X4 Pin	Device Pin	Function		X4 Pin	Device Pin	Function
1		VCC		26		GND
2		GND		27	B1	D2A
3	B7	D4A		28	D3	D2B
4	A6	D4B		29	E2	D2C
5	A5	D4C		30	C1	D2D
6	C6	D4D		31	E3	D2E
7	B6	D4E		32	D1	D2F
8	A4	D4F		33		VCC
9		VCC		34		GND
10		GND		35	F2	D2G
11	A3	D4G		36	E1	D2col
12	A2	D4dp		37	F1	D2dp
13	C5	D4col		38	G2	D1A
14	B5	D3A		39	F3	D1B
15	B4	D3B		40	H2	D1C
16	C4	D3C		41		VCC
17		VCC		42		GND
18		GND		43	H3	D1D
19	C3	D3D		44	G3	D1E
20	C2	D3E		45	G1	D1F
21	B3	D3F		46	H1	D1G
22	B2	D3G		47	J2	D1col
23	A1	D3dp		48	J3	D1dp
24	D2	D3col		49		VCC
25		VCC		50		GND

Table 5. X4 Pin connections

7. JTAG - Interface

The JTAG interface can be used for In-System Programming and for Boundary Scan Test. X5 corresponds to the standard Lattice Download cable pinout (see table 6).

After programming you should reset the device to ensure proper operation. For details on In-System Programming and Boundary Scan Test, please refer to the Lattice documentation or the Lattice homepage (www.latticesemi.com).

X5 Pin	Device Pin	Function
1		VCC
2	G14	TDO
3	K3	TDI
4	NC	
5	NC	
6	J1	TMS
7		GND
8	K2	TCK

Table 6. X5 Pin connections (JTAG-Port)

8. Jumper settings

Here you find a brief summary of the jumper settings:

Jumper	Function	Factory setting
Y1	connects VCCIO-Pin to VCC(3.3V)	ON
Y2	connects VCCIO-Pin to X6, Pin 11	OFF
Y3	connects CLK2-Pin to on-board Oscillator	ON
Y4	connects CLK2-Pin to X6, Pin 5	OFF
Y5	pulls TOE / I/O 0 to GND	OFF

Table 7. Jumper settings

CAUTION: Do not feed an external clock signal to X6, pin5 with both Y3 and Y4 set. You will probably kill your clock source, the onboard-oscillator or both!

CAUTION: Do not feed external 2.5V with Jumpers Y1 and Y2 both set! Set Y1 for VCCIO = 3.3V (from on-board supply) or set Y2 for VCCIO = 2.5V (connect a 2.5V / 30mA - supply to X6, Pin 11).

9. Accessories, stuff you may need

You need some kind of software to produce the JEDEC-Files for the ispLSI5256VA. At the time, this manual is written, a starter-software is available free of charge from Lattice Semiconductors homepage (www.latticesemi.com).

Software, which supports VHDL or Verilog can be purchased for a few hundred dollars, which is a good investment. With any Software you buy from Lattice you get a download-cable. The download-cable can be purchased separately for less than $100.-- at any Lattice Representative or Distributor. The order-code is: PDS4102-DL2

10. Application Examples, Support

Application examples for this demoboard can be downloaded from our homepage: www.bosshard-elektronik.ch
If you do an interesting, funny, useful, strange or smart application we would be happy to receive a copy. Please include your approval or denial to post your application on our homepage.

Customized versions of the Demoboard are possible:

- ispLSI5256VA in BGA208 with different speed-grades
- ispLSI5384VA in BGA208, all available speed grades
- different frequencies for the on-board oscillator
- customized silk-screen

Please contact sales@bosshard-elektronik.ch for pricing / lead-times.

Support for any **demoboard-related issues** can be obtained by contacting
support@bosshard-elektronik.ch .

Please do not request our support for issues concerning design-software or the ispLSI5256VA - device. This is supported by the Lattice Representatives or Distributors in your area.

11. Specifications

Parameter	MIN.	NOMINAL	MAX.	UNITS
Supply Voltage	4.75	5.0	6.0	V
Current Consumption			1.0	A
VCCIO (optional)	2.3	2.5	2.7	V
Current needed for VCCIO Pin			30	mA
Voltage available at VCCout (X7)	3.2	3.3	3.4	V
Current available from VCCout	100			mA
Operating Temperature	0		70	°C
Physical Dimension		100 x 160		mm

12. Additional comments

Our boards are much better than our english.
Any suggestions for improvements on this document are highly welcome. Please email to: demoboard@bosshard-elektronik.ch .